Reply to Office Action of February 9, 2006

## Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

- 1. (Original) A closed cell trench metal-oxide-semiconductor field effect transistor (TMOSFET) comprising:
  - a drain region;
  - a body region disposed above said drain region;
  - a gate region disposed within said body region;
  - a gate insulator region disposed about a periphery of said gate region;
- a plurality of source regions disposed along the surface of said body region proximate a periphery of said gate insulator region;

wherein a first portion of said gate region and a first portion of said gate insulator region are formed as a substantially parallel elongated structure;

wherein a second portion of said gate region and a second portion of said gate insulator region are formed as a normal-to-parallel structure;

wherein a first portion of said drain region overlaps said parallel structure; and

wherein a second portion of said drain region is separated from said normalto-parallel structure.

Appl. No. 10/726,922

Amdt. Dated

Reply to Office Action of February 9, 2006

2. (Original) The closed cell TMOSFET according to Claim 1, wherein said closed cell MOSFET provides a low gate-to-drain capacitance (Cgd) on resistance (Rds-on) product.

3. (Original) The closed cell TMOSFET according to Claim 1, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio.

4. (Original) The closed cell TMOSFET according to Claim 1, wherein said overlap of said first portion of said drain region and said parallel elongated structure comprises an extension of said drain region.

- 5. (Original) The closed cell TMOSFET according to Claim 1, wherein said separation of said second portion of said drain region and said normal-to-parallel elongated structure comprises a well of said body region.
- 6. (Original) The closed cell TMOSFET according to Claim 1, wherein said body region and said plurality of source regions are electrically coupled together.

7. (Original) The closed cell TMOSFET according to Claim 1, wherein;

said drain region comprises an n-doped semiconductor;

said body region comprises a p-doped semiconductor;

said gate insulator region comprises an oxide;

said plurality of source regions comprise a heavily n-doped semiconductor;

and

said gate region comprises a heavily n-doped semiconductor.

8. (Original) The closed cell TMOSFET according to Claim 1, wherein said drain region comprises:

a first drain portion having a high doping concentration; and

a second drain portion, having a low doping concentration, disposed between said body region and said first drain portion.

- 9. (Original) The closed cell TMOSFET according to Claim 8, wherein said second drain portion increases a reverse breakdown voltage of said closed cell TMOSFET.
  - 10. (Original) The closed cell TMOSFET according to Claim 8, wherein:

Appl. No. 10/726,922

Amdt. Dated

Reply to Office Action of February 9, 2006

said first portion of said drain region comprises a heavily n-doped semiconductor; and

said second portion of said drain region comprises a lightly n-doped semiconductor.

11-23 (Canceled).

24. (Original) A closed cell trench metal-oxide-semiconductor field effect transistor (TMOSFET) comprising:

a plurality of open gate-drain regions arranged in a first plurality of parallel regions; and a plurality of closed gate-drain regions arranged in a second plurality of parallel regions normal to said open gate-drain regions.

25. (Original) The closed cell TMOSFET according to Claim 24, wherein the combination of said plurality of open gate-drain regions and said plurality of closed gate-drain regions reduces the gate-to-drain capacitance (Cgd) on resistance (Rdson) product.

26. (Original) The closed cell TMOSFET according to Claim 24, wherein the combination of said plurality of open gate-drain regions and said plurality of closed

Appl. No. 10/726,922 Amdt. Dated Reply to Office Action of February 9, 2006

gate-drain regions reduces the gate-to-drain capacitance gate-to-source capacitance ratio.